

FAB NOTES:

1. ALL DIMENSIONS ARE IN INCHES, UNLESS OTHERWISE NOTED.
2. THE PWB SHALL BE FABRICATED TO IPC-6012, CLASS 2, AND WORKMANSHIP SHALL CONFORM TO IPC-A-600, CLASS 2; CURRENT REVISIONS.
3. BOARD MATERIAL SHALL BE 180 Tg/350 Td ISOLA FR-370HR OR EQUIVALENT, R6HS COMPLIANT AND LEAD FREE ASSEMBLY CAPABLE. BOARD MATERIAL SHALL MEET OR EXCEED IPC-4101B, COLOR: NATURAL.
4. BOARD MATERIAL & CONSTRUCTION TO BE U.L. APPROVED AND MARKED ON THE FINISHED BOARD.
5. MINIMUM COPPER WALL THICKNESS OF PLATED-THRU HOLES TO BE .001 INCH, WITH A MINIMUM ANNULAR RING OF .002 INCH.
6. OVERALL BOARD THICKNESS TO BE .062 +/- .01% AND APPLIES AFTER ALL LAMINATION AND PLATING PROCESSES - MEASURED FROM COPPER TO COPPER.
7. MAX. WARP & TWIST TO BE .0075 INCHES PER INCH.
8. BOARD MUST BE ELECTRICALLY TESTED USING SUPPLIED IPC-D-356 NETLIST.
9. PLATED THROUGH SLOT INDICATED WITH MULTIPLE DRILL HITS SHOULD BE
10. ALL VIAS TO HAVE SOLDERMASK.

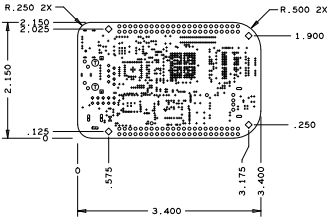
FINISHED AS SMOOTH WALL BY VEDOR.  
PROCESS NOTES:

1. PLATE ALL EXPOSED AREAS WITH ELECTROLESS IMMERSION GOLD, NICKEL 150 MICROINCHES THK MIN GOLD 5-15 MICROINCHES THK MIN.
2. APPLY LP1 SOLDERMASK OVER BARE COPPER (SMD0C), COLOR: BONE OR OFF WHITE. SOLDERMASK SHALL CONFORM TO IPC-SM-840, CLASS H, CURRENT REV.
3. SOLDERMASK ARTWORK HAS ZERO (0) OVERSIZED PADS. FABRICATION VENDOR IS ALLOWED TO ADJUST THE COMPONENT SOLDERMASK PADS TO MEET THEIR TOOLING REQUIREMENTS.
4. APPLY LP1 SILKSCREEN OR EQUIVALENT PER THE ARTWORK. COLOR: BLACK.

DRILL CHART: TOP 1x BOTTOM					
ALL UNITS ARE IN MILS					
FIGURE	SIZE	TOLERANCE	PLATED	QTY	
1	8.0	+3.0/-3.0	PLATED	199	
2	12.0	+3.0/-3.0	PLATED	28	
3	38.0	+3.0/-3.0	PLATED	18	
4	40.0	+3.0/-3.0	PLATED	102	
5	63.0	+3.0/-3.0	PLATED	2	
6	125.0	+3.0/-3.0	PLATED	4	
7	30.0	+5.0/-5.0	NON-PLATED	1	
8	128.0	+5.0/-5.0	NON-PLATED	2	
9	95.0x40.0	+3.0/-3.0	PLATED	2	
10	120.0x40.0	+3.0/-3.0	PLATED	1	
11	120.0x40.0	+3.0/-3.0	PLATED	1	
12	140.0x40.0	+3.0/-3.0	PLATED	1	

LAYER STACK-UP - ALL DIMENSIONS IN INCHES

LAYER#	COPPER WEIGHT (oz)	50um SINGLE ENDED IMPEDANCE CONTROL +/- 10%		50um DIFFERENTIAL IMPEDANCE CONTROL +/- 10%		100um DIFFERENTIAL IMPEDANCE CONTROL +/- 10%	
		TRACE WIDTH	SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE	TRACE WIDTH / SPACE
LAYER 1 - PRIMARY SIDE - SIGNAL	HALF-PLATING	4.75		4.5/6.5		3.75/7.25	
LAYER 2 - GROUND PLANE	1						
LAYER 3 - SIGNAL	1	5.25		5.0/7.0		4.00/8.00	
LAYER 4 - SIGNAL	1	5.25		5.0/7.0		4.00/8.00	
LAYER 5 - SPLIT POWER PLANE	1						
LAYER 6 - SECONDARY SIDE - SIGNAL	HALF-PLATING	4.75		4.5/6.5		3.75/7.25	



APPROVED		CIRCUITCO.	
CHECKED			
DRAFTING	CalCad	FABRICATION DRAWING, BEAGLE BONE	
DATE	02/22/12	ENGR	TOLERANCES UNLESS OTHERWISE SPECIFIED
DESIGN ENGR			
PROJECT ENGR			
ENGR MGR			
NEXT ASSEMBLY		DO NOT SCALE DRAWING	
		SCALE	NONE
		SHEET	1 OF 1
		PCB REV	C2
		SURE	D